Hall Ticket Number:

Code No.: 6126 M

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. I Year (ECE) I-Semester (Make Up) Examinations, March-2016

(Embedded Systems & VLSI Design)

VLSI Technology

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** questions from **Part-B***

Part-A (10 X 2=20 Marks)

1. Explain the reason why it is difficult integrate inductors on ICs?
2. Describe the isolation technique used in CMOS ICs.
3. Discuss the advantages of silicon as the base material for IC processing.
4. Explain the need to form oxide layers by deposition only, after gate electrode formation in CMOS process.
5. Explain the importance of epitaxial layers in ICs.
6. Explain the importance of wafer cleaning before each process step.
7. Indicate the advantages of dry etching over wet etching.
8. Indicate the merits of contact / proximity exposure from resolution point of view.
9. Describe the advantages of Ion Implantation over Diffusion.
10. Indicate various types of testing carried out on VLSI chips.

Part-B (5 X 10=50 Marks)

11. a) Describe the various isolation techniques that are used in ICs and discuss their relative merits and demerits. (6)
    b) Explain two different structures of capacitors realized on ICs. (4)

12. a) Discuss the functionality of poly silicon, thin oxide and thick oxide layers in CMOS ICs. (5)
    b) Explain what is meant by self-aligned gate structure and explain how it is formed. (5)

13. a) Discuss the Oxidation rate dependency on Orientation. (3)
    b) Briefly describe the Molecular beam epitaxial process and discuss its advantages and disadvantages. (7)

14. a) Discuss the various issues related to deposition of thin films in VLSI processing. (5)
    b) Compare the LPCVD and PECVD techniques of depositing thin films. (5)

15. a) Discuss the dependency of range and standard deviation of an implanted species on implantation energy and implanted species. (7)
    b) Discuss the temperature dependency of the Diffusivity. (3)

16. a) Explain what is BICMOS process is and discuss the additional steps that are required to be added to a normal CMOS process to convert it to a BICMOS process. (6)
    b) Explain the auto doping effects in vapor phase epitaxy. (4)

17. a) An n well of 4 microns depth has to be formed in a CMOS process using phosphorous. The doping concentration required is 10^{17} P atoms / cm^3. Calculate the implant dose (ions/cm^2) required. (4)
    b) Explain how junctions are formed using multiple diffusions illustrating with an example? (6)

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